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Research paper

Characterization of silane based ultra-thin barrier deposited at elevated temperature

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ABSTRACT

In this work, we describe a quick turn-around characterization approach of ultra-thin layers on low dielectric constant (Low-K) interlevel dielectric using Electrochemical Impedance Spectroscopy (EIS). It is demonstrated on an organo-silane based ultra-thin Cu barrier layer, deposited from liquid phase at elevated temperatures, 90 °C - 150 °C, using high flash temperature solvents: *N*-methyl-2-pyrrolydone (NMP, $T_{flash\text{-}point}$ = 91 °C) or Ethylene glycol (EG, $T_{flash\text{-}point}$ = 116 °C). Three Silane (Head group) based monomers; with three different tail groups (e.g. amine, aniline and methacrylate) were investigated; The elevated temperature deposition process allowed shorter deposition times (less than 15 min), compared to previous publications. Additionally, the high flash point solvents reduce the risk of spontaneous explosion or ignition. All three monomers yielded satisfactory barrier against copper transport, being tested for more than 10 h at temperature higher than 400 °C, on all substrates. The need for a quick turn-around and a simple way to determine the barrier presence, its thickness and its coverage, lead to explore the application of Electrochemical Impedance Spectroscopy (EIS). We demonstrate the capability of that method estimating thickness and coverage of such ultra-thin barriers deposited on relatively thick (~200 nm) Low-K dielectric materials. It was found that EIS below 10 Hz at negative wafer bias vs. the electrolyte reference, the impedance real part was affected by the ultra-thin layer on thick dielectric materials allowing to define an Effective Electrical Coverage (EEC) of the films on Low-K dielectric similar to what has already been defined on bare silicon. The EEC is a figure of merit and its relation to the actual surface coverage, and barrier properties, is briefly discussed.

1. Introduction

Ultra-thin layers (UTL), either ordered, such as Self Assembled Monolayers (SAM), or unordered, with an average thickness in the order of 1–2 nm, are candidates for various applications in micro-system technologies. For example, they are used for adhesion and barrier layers [1–3] for advanced processes for Very Large-Scale Integration (VLSI) of Integrated Circuits (ICs). Currently the critical dimensions of the main features, i.e. gates, contacts and interconnects, of advanced ICs have shrank to below 10 nm; Hence there is not much room at the bottom for auxiliary layers (e.g. barrier, adhesion and capping layers) that are needed for reliability and integrity considerations.

Nanoscale copper interconnects have few critical issues due to their size. There are the intrinsic problems where the large surface to volume ratio and the narrow linewidth affect the line resistivity and reliability. There are also extrinsic problems due their interaction with the inter-level dielectric or the semiconductor devices, i.e., contact effect, delamination, and copper transport onto the interlevel dielectric. Recent solution to those issue ranges from replacing copper with cobalt in the contacts or keeping the copper and using Ultra-thin layers between the copper and the Inter Level Dielectric (ILD) [4,5]; The Ultra-thin layers can be deposited either by Atomic Layer Deposition (ALD) or by Liquid Phase Deposition of Self-Assembled Ultra-thin layers [6–16].

Atomic or molecular thick layers should be uniform, defect free, with full coverage and low effective dielectric constant in order to avoid an increase of the parasitic capacitance. Maintaining low capacitance is

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important since it directly affects the interconnect network speed, cross talk and power consumption. Carbon-based ultra-thin layers that have low polarization have lower effective dielectric constant over commonly used ALD films (i.e. TiO_2, Al_2O_3, or HfO_2); therefore, carbon based Ultra-thin layers technology may offer better delay time when compared to that of metal-oxides.

In this paper we present results from samples with ultra-thin barriers deposited at the liquid phase from high flash point solvents using silane-based monomers with a short intermediate chain (between the tail and the head groups) of 3 carbon atoms (e.g. propyl), connecting the head and tail groups and the deposition time is rather short, less than 30 min. Note that we use monomers with a longer chain to get the best lateral assembly and to deposit at longer times, up to few hours, in order to get better coverage. However, the film thickness depends on the silane intermediate chain and for VLSI barrier applications the need is to make it as thin as possible, in the ~1 nm range. Therefore, we explore a propyl-silane based monomers assuming that even without large scale lateral assembly the ultra-thin film will be a good barrier.

Silane based ultra-thin copper barriers have already been demonstrated; they usually referred as Self Assembled Monolayers (SAM), although the level of assembly is limited, and the structure includes also significant amount of disorder. Typically, Organo-silane molecules are used since the monomers head-group (e.g. silicon-tri-methoxy) reacts with the substrate forming a stable bond. The bound molecules can form a self-assembled 2-D periodic structure, or a random network of molecules entangled to one another forming an ultra-thin layer with a thickness of order of the molecule length. Typically, in fully assembled monolayers, the layer thickness is calculated as the molecular length times the cosines of the average angle of inclination (taken from the normal) of the molecule relative to the surface. Nowadays, the monomers are typically deposited using organic solvents, either polar (i.e. ethanol, IPA) or non-polar (i.e. toluene). Those solvents that are being used have relatively low flash-point temperatures, $\leq 70\,^{\circ}C$; Hence it may pose a safety hazard in manufacturing since the deposition bath can be ignited or explode spontaneously. Ultra-low thin film liquid phase depositing at low temperature using the reaction between the silane groups and the dielectric can be a long process, which may take hours. Therefore, the cost effectiveness and applicability of this process in mass production is a serious concern. One option is to use a batch process. Another potential solution to accelerate the deposition is by introducing other solvents with higher ($>90\,^{\circ}C$) flash-point temperatures, allowing the liquid phase deposition process at higher temperatures. We demonstrate a good silane-based barrier deposited from solvents such as *N*-Methyl-2-pyrrolidone (NMP) and Ethylene glycol (EG) at temperatures of up to 150 °C; Those processes offer a safer and faster deposition \ compared to those with ethanol or toluene-based bathes.

We present here the results of a feasibility study of the silane-based ultra-thin layers, in the range of one molecular length, deposited at relatively elevated temperatures directly on single crystal silicon (100) and on thin dielectric materials on similar substrate. Three different ultra-thin layers were deposited using the same silane head group, the same propyl chain, and with three different tail groups studying its effect on the barrier properties.

There are many ways to characterize ultra-thin layers on various substrate. For example, one can count TEM, XRR and Ellipsometry for the layer thickness and XPS or AES for the layer thickness and chemical analysis. Regarding the thickness measurement TEM analysis can be used giving direct evidence of the layer, however it is expensive, slow, with long turnaround time providing information on very small sampling area (less than micron) which is a problem when we test an ultra-thin layer on a 30 cm diameter wafer. XRR is also an alternative for the thickness evaluation, however, it is model dependent and the results on Low-K dielectric are very often different than that of the TEM. Ellipsometry is another option, yielding data on the whole wafer although the results are model dependent and require calibration.

One of the key problems in characterizing ultra-thin layers is related to the defects: pinholes and local disorders in the ultra-thin layers and incomplete surface coverage. Those defects can form a path for copper transport affecting the barrier properties. Defect characterization by high resolution electron microscopy is very tedious, requiring first finding the defects and second, its high-resolution imaging and analysis. Therefore, using TEM, for inline defect characterization in ultra-thin layer can be a problem. In this paper we discuss two alternative ways. The first is Kelvin Probe Scanning Force Microscopy (KPFM) which yields an aerial image of defects (among other features) that are affecting the surface potential. Another method is the Electrochemical Impedance Spectroscopy (EIS) at variable bias. EIS is an indirect method based on electrical model that is representing the various layers; therefore, it yields an effective surface coverage. The results for the deposited layers on silicon has already been published following a conventional electrical coverage modeling [17]. However, applying the same methods to ultra-thin layers on a thick low-K dielectric generate a very low signal (i.e. impedance variations due to the ultra-thin film presence) since the low-K capacitance is much lower than the serial capacitance of the ultra-thin layer and its electrical resistance is assumed to be much higher. Therefore, the impedance of the low-K is assumed to be much higher than that of the ultra-thin layer. Other electrochemical methods such as cyclic voltammetry have been used for detection of barrier defects for copper interconnect on low-k. The Cu reaction peak current is used as an indicator for barrier defect: When the barrier is defective, the hysteresis current is much higher than the capacitive current [18].

However, analyzing EIS measurements at accumulation yields new results. It was found that in accumulation at low frequencies, the impedance phase was close to zero degrees (i.e. resistive) indicating on some conduction mechanism via the porous oxide. Assuming that the impedance depends on the surface converge, this allowed us to calculate the effective electrical coverage using rather simple model. However, note that the electrical effective coverage depends on the defect density as well as the spacing between the molecules. Therefore, the effective electrical coverage is not identical to the material coverage. However, both depend on the defect density, therefore, we assume that they can both serve as indicators to the barrier properties.

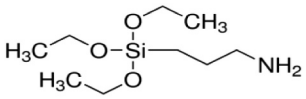
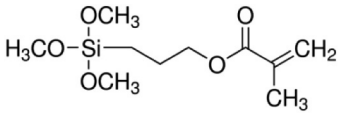
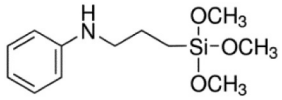
2. Experimental

The study was conducted using single crystal Si wafers (P type, (100)). The layers were deposited on a. bare Si, b. Si covered by 6 nm thick thermal oxide and c. Si covered by a porous Low-K dielectric (200 nm thick, proprietary MSQ type). The samples were initially cleaned by the RCA-1 process, e.g. $NH_4OH{:}H_2O_2{:}H_2O$ = 1:1:6 (volume ratio) at 85 °C for 20 min [19]; removing organic residues. Next, only bare Si and SiO_2 samples were dipped for ~1 min in hydrofluoric acid 2% aqueous solution at room temperature the remove native oxide. Finally, all the samples were rinsed and dried (in air) twice: first in C_2H_5OH (e.g. Ethanol absolute) and the second in the solvent under study (e.g. NMP or EG).

The Silanization process was performed in closed vials containing 1% of the silane monomer in the solvent. The following precursors were used (see Table 1): (a) Aminopropyltriethoxysilane (UTL-1), (b) 3-(Trimethoxysilyl) propyl methacrylate (UTL-2), (c) N-[3-(Triethoxysilyl)-propyl] aniline (UTL-3); all purchased from Sigma-Aldridge. Two solvents have been studied: (a) NMP- (N methyl-2-pyrrolydone, C_5H_9NO) and (b) EG- (Ethylene glycol $C_2H_6O_2$). The Silanization process was performed for 1–15 min at 105 °C, 125 °C and 150 °C. The deposition temperature was stabilized using a temperature-controlled heating bath with either ethylene glycol or glycerol. Following the Silanization, the samples were washed under ultrasonic agitation; first in ethanol and next in isopropanol (30 min each step). Finally, the samples were dried with N_2 gas stream and oven baked at 100 °C in air for 30 min to stabilize the ultra-thin layers and remove any solvent residue.

Following Silanization, few samples were coated by 100 nm thick

Table 1
Chemical formulas and nomenclature of the ultra-thin layers used in this work.

IUPAC name	M, g/mol	Formula	Molecule
3-Aminopropyltriethoxysilane (APTES)	221.37		UTL-1
3-(Trimethoxysilyl) propylmethacrylate	248.35		UTL-2
N-[3-(Trimethoxysilyl)propyl] aniline.	255.39		UTL-3

copper for further barrier study. The copper was deposited by PVD (*E*-beam evaporation at 70–80 μTorrs) at low deposition rate, about 0.5 to 1 Å/s to minimize surface damage.

After evaporating the Cu on the Ultra-Thin-Layers (UTLs), a metal-oxide semiconductor (MOS) based structures is formed, in order to use UTLs in molecular electronics or hybrid electronics, it is essential that UTLs must remain intact under the same conditions that all existing semiconductor materials already endure. These include thermal stability, therefore MOS structure have been subjected to stability test under certain condition, which includes high temperature in a vacuum (annealing)- so-called barrier test.

It is known that Cu diffuses fast in Si and forms Cu-Si compounds at a temperature as low as 200 °C. The formation of copper silicide is monitored by resistivity measurements of the Cu/barrier/Si stack. The barrier effectiveness was tested on samples that passed vacuum annealing at 10^{-6} Torr, at 525 °C for different periods of time ranging from 10 min to 670 min. This method was an indicator for the stability of the barrier layer since copper-silicide formation results in a drastic increase of resistivity of Cu films as silicide has a higher resistivity than copper.

The sheet resistance of the Si/barrier/Cu structure was measured, after each period of annealing, by a four-point-probe system, Jandel Engineering Ltd. model RM3000. This system consists of four (in-line) equally spaced (1 mm) tungsten metal tips. A high impedance current source was used to supply current of 1 mA through the outer two probes while a voltmeter measures the voltage across the inner two probes to determine the sample resistivity.

The rest of the samples were taken to physical and chemical analysis such as Contact Angel (CA) and Spectroscopic Ellipsometry and Kelvin Probe Scanning Microscopy (KPFM). More details about the equipment used and their error margins of the equipment can be found in the Supplementary material (Section S1).

Electrochemical Impedance Spectroscopy (EIS) in a 1 M potassium nitrate (KNO_3) aqueous solution was the method chosen for electrical characterization, which also gives information of the layer coverage and integrity. An Ohmic contact was prepared to the sample by: (a) native oxide removal by a 2% HF in water dip etch followed by rubbing Gallium-Indium eutectic $\geq$ 99.99% trace metals basis (Sigma-Aldrich) on the sample backside. The measurements were performed using a homemade O-ring cell using a homemade Teflon apparatus with a well-defined semiconductor area exposed to a potassium nitrate (KNO_3) 1 M aqueous solution. The impedance was measured using potentiostat/galvanostat (VSP®, BioLogic Science Instruments Ltd.) at the 0.1–10^5 Hz range. That specific solution was chosen since it keeps the surface stable under that measurement conditions. The sample were sealed by a Teflon cell with a circular area with a diameter of 7 mm (area of 0.385 cm^2). The system was set-up with Pt wire as counter electrode (CE) and Ag/AgCl homemade reference electrode (RE). The Ag/AgCl homemade reference electrode stability was calibrated versus commercial Ag/AgCl (Saturated KCl) electrodes, which was found to be stable with very low drift [20].

3. Results and discussion

3.1. Contact angle

Contact angle measurements verified the effect of the layers' presence on the samples' surface. For example, the results for three ultra-thin layers using NMP deposited at 125 °C, 12 min. Are shown in (Supplementary materials Fig. S1) for either thermal oxide or a reference bare Si. The contacts angle for bare Si was 59.8° ± 1° [21], while after Silanization it was 67.5°, 47.0° and 42.3° for the UTL-1,2 & 3 respectively. The process effect on the oxide was more pronounced with an increase of the contact angle from about 22.5° to near 50° for all the layers indicating on the surface functionalization [22–24].

3.2. Ellipsometry

Ellipsometry for layers on Si yielded a ~3 nm thick layer for UTL-1, ~2 nm for UTL-2 &UTL-3. Those measured values are slightly higher than the expected and measured thickness [23–25]. Therefore, it is assumed that those values include also the native oxide between the ultra-thin layers and Si. Ellipsometry results on thermal oxide and the Low-K dielectric were less conclusive, probably due to a. the small difference in the refractive index between the Ultra-thin layers and the dielectric material and also due to the fact that solvent and some organic residue are attracted to defects and pores on the dielectric materials changing its top layer optical properties.

3.3. Kelvin probe scanning microscopy (KPFM)

The KPFM spectrum shown in (Supplementary materials Fig. S2) demonstrates the capability of this method to present nanoscale information about the thin film structure. This figure shows that the KPFM image verifies the presence of the ultra-thin layer and its 2D granular structure. The layers are composed of thin island surrounded by a dark boundary line which is due to either local charge or oxide thickness variation. One way or another we can assume is related to the 2D grain boundary. The information from the KPFM (Surface Potential) was compared to the AFM image (topography), and as shown in (Supplementary materials Fig. S2) the KPFM image contains significantly more details. The main disadvantage of the scanning probe method is that it requires a long setup time to overcome initial charging and the scan rate itself is rather slow, about 3 h per sample at the highest resolution.

3.4. Electrochemical impedance spectroscopy (EIS)

First, we did study the elevated temperature layers deposited directly

on silicon (Fig. 1). At negative bias, when the ultra-thin layer/Si device was at accumulation (It is a p-type silicon, therefore holes are attracted to the surface under negative bias on the gate), the device behaved like the silicon impedance (e.g. accumulation capacitance) in series to the ultra-thin-layer capacitance in series to the Randle's model [17,26]. The model capacitance, measured at the intermediate frequency range, was about 3 μF/cm^2 which can be attributed to the double layer capacitance in series to the ultra-thin capacitance (neglecting the silicon accumulation capacitance which is much higher). At low frequency the impedance real part was dominant and dominated by the contact resistance (R_{ct}) which was typically in the range of slightly above 10^5 Ohms. samples without the ultra-thin showed similar characteristics, however, with significantly lower R_{ct} at lower frequency and slightly higher impedance at the intermediate regime. The difference between the samples with the ultra-thin layers to those without the ultra-thin layers can be attributed to the ultra-thin layer effective coverage [17].

At positive bias (Fig. 1) the capacitor is under inversion, and the silicon impedance is not negligible. We observed both the inversion and depletion capacitance at low frequency, the depletion capacitance at the high frequency. The silicon impedance transition from low to high frequency was also a function of the equivalent resistance representing the contribution of the generation current according to the Shockley-Read-Hall model at the depletion layer [26,27].

Increasing the bias induces the formation of the depletion layer at about −0.2 V and later the inversion layer at positive bias. This causes adding a serial semiconductor impedance that includes the double layer capacitance, the inversion layer capacitance and the effective generation-recombination resistance in series to the inversion layer capacitance. This is demonstrated by the appearance of a second pole at higher frequency that is shifted to lower and lower frequencies as the bias increases as expected by conventional MOS capacitor AC impedance models (See for example [27,28]).

The coverage of ultra-thin-layer on silicon wafer directly is calculated from the resistance at low frequency. The assumption from this range was that without ultra-thin the low frequency resistance is only the charge transfer resistance, R_{ct}. With ultra-thin layer there is the serial resistance of the ultra-thin layer, R_{UTL}, which is much higher. Therefore, the total resistance is supposed to be:

$$\frac{1}{R} = \frac{1-x}{R_{ct}} + \frac{x}{R_{ct}+R_{UTL}} \approx \frac{1-x}{R_{ct}} + \frac{x}{R_{UTL}} \tag{1}$$

Assuming $R_{UTL} \gg R_{ct}$. Hence, the effective electrical coverage, x, can be estimated as:

$$x \cong 1 - \frac{R_{ct}}{R_{UTL}} \tag{2}$$

The effective coverage, x, calculated from the data shown in Fig. 2 (at-0.6 V) is about 95.1%. A better estimate can be deduced by taking the data in the larger bias range of −0.6 V to −0.2 V. In this range the value of x was calculated to be 91.3 ± 2.7%.

The coverage affects also the capacitance as shown in the impedance in the midrange, ~100 Hz to 1KHz. In that range, under negative bias, we can assume that the semiconductor is in accumulation, its serial capacitance is very high and, therefore, negligible compared to the serial double layer and the ultra-thin layer capacitance. Therefore, we can calculate the total capacitance is the double layer capacitance of the uncovered area in parallel to the double layer capacitance in series to the ultra-thin layer capacitance of the covered area:

$$C = (1-x)C_{dl} + x\frac{C_{dl}\cdot C_{UTL}}{C_{dl}+C_{UTL}} \tag{3}$$

The coverage estimation from that equation is:

$$x = \left(1 - \frac{C}{C_{dl}}\right)\cdot\left(1 + \frac{C_{ML}}{C_{dl}}\right) \tag{4}$$

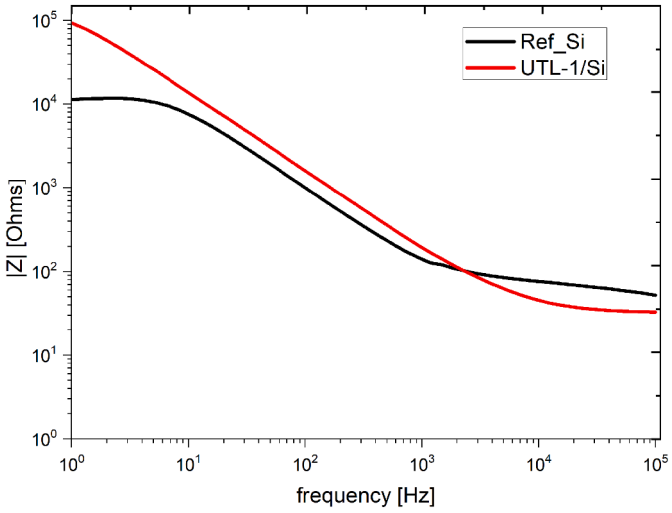


Fig. 2. EIS of UTL-1/Si and on Si only at accumulation (−0.6 V).

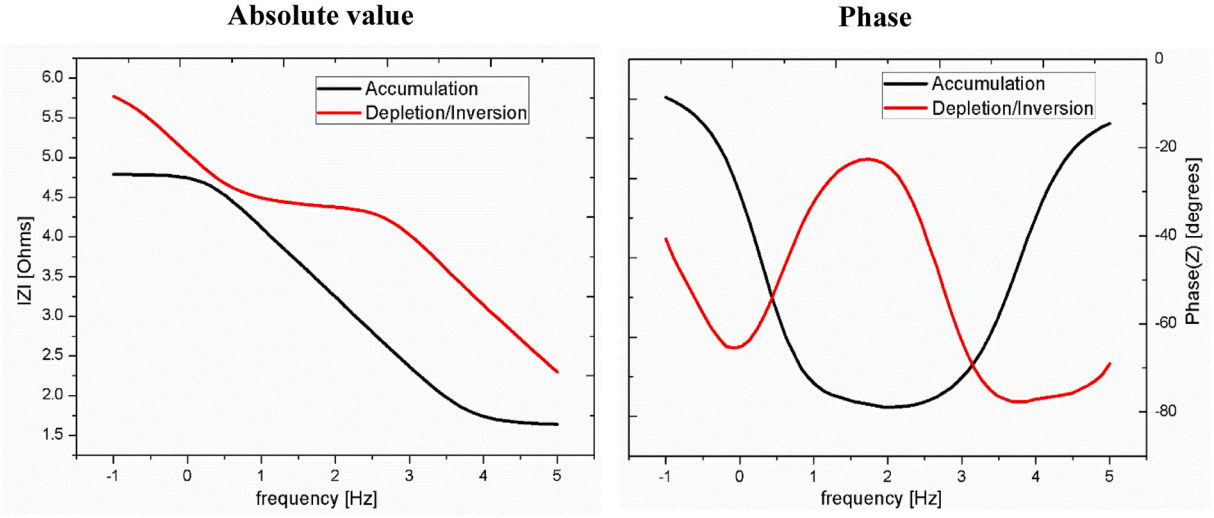


Fig. 1. EIS of UTL-1/Si at Accumulation (−0.6 V) and inversion (+0.6 V).

where C is the measured capacitance with the ultra-thin layer and C_{dl} is the double layer capacitance which is the capacitance without the ultra-thin layer. The problem in that equation is that we have two variables, C_{UTL}, and x the coverage. Therefore, we cannot calculate the coverage in this case form the capacitance, unless we estimate the value of the ultra-thin layer capacitance relative to the double layer capacitance. An alternative is to take the effective x from the resistance measurement. Taking x = 91.3% we find $\frac{C_{UTL}}{C_{dl}} \approx 1.3 \mp 0.2$.

Next, we present the results of the ultra-thin layer measurement on samples with ultra-thin layer on the porous Low-K interlevel dielectric (Fig. 3).

First, it is clear that the sample on Si show a notable different plot than those on the Low-K, indicating on a larger capacitance at the mid frequency range. Next, as expected, in the inversion regime (roughly above −0.3 V) all the plots of the impedance of samples with and without ultra-thin layer on the Low-K/Si where almost the same with purely capacitive characteristics with almost the same value. This is expected since the ultra-thin layer thickness is in the range of ~1 nm while the porous Low-K dielectric is ~200 nm. There is a slight increase of the impedance after the ultra-thin layer deposition, however, since there are also sample-to-sample variations an attempt to estimate the ultra-thin layer capacitance and the coverage form the impedance at the midrange, similar to what we demonstrated for the ultra-thin layer/Si before (Eq. 1–4) yields relatively large error. The phase peak (in the range of 10-100 Hz) of the samples with the ultra-thin layer/Low-K also shows a slight shift to lower values that can be attributed to an additional serial capacitance. However, also in this case the data is rather noisy. Therefore, the only thing that can be deduced from this data is that there is an additional capacitance, probably due to either ultra-thin layer on top or an increase of the dielectric capacitance due to penetration of ultra-thin layer monomers onto its pores.

The overall Impedance of the deice is shown as a function of the frequency at different bias, starting from relatively large negative gate bias (−1.8 V) to positive (Fig. 3). That impedance can be described by the model shown in Fig. 4 which assumes that the covered area impedance is in parallel to the uncovered regime. The results indicated that impedance of the samples with the ultra-thin layer is higher than that without the ultra-thin layer; thus, the presence of the ultra-thin layers verified.

At low frequency, we observed a dominant real value of the impedance only under accumulation; for bias < -1.5 V. Under those conditions, the low-k dielectric conductivity, $G_{LowK} = Re\{Y\}$, becomes larger than the imaginary part value of the Low-K admittance, ($Im\{Y\} = 2\pi f C_{LowK}$). At higher bias, the impedance becomes mostly capacitive and at 0 V bias or above there is almost no difference (at low frequency) between the characteristics of the various samples. All those impedance characteristics, at 0 V bias or above, converge to that of the reference Low-K/Silicon.

We can see that at high frequency the capacitance is dominated by the low-K capacitance which is about 6 nF (or ~ 15 nF/cm^2). This also means that at high frequency when the Low-K capacitance becomes dominant and there is no leakage due to the high bias. Since we exclude electrical leakage via the low-K dielectric we may assume that the conduction at negative bias, <-1.5 V, is due to ionic conducting in the low-K. we can also assume that the ions penetrate via pinholes, defects and uncovered regions in the ultra-thin films. The ions can also penetrate via the space between the film molecules.

Below ~10 Hz the impedance becomes real and can be represented as a resistor. After the ultra-thin-layer deposition that resistance increases, probably due to the coverage of the ultra-thin layer. As before, we can assume an effective electrical coverage, x. This is probably due to the ionic conduction of the protons or the hydroxyl ions inside the porous material.

Assuming that the ultra-thin layer passivates the Low-K material we can calculate the coverage using the same expression as before (Eq. 1). Since the signal is very noisy at 0.1 Hz, due to external interference, we calculate the coverage from the data at the frequency range between 1 and 5 Hz (Table 2). This table shows that the tail group plays an important role on the effective electrical coverage of the ultra-thin layer. This emerges from both amplitude and phase measurements at the negative bias range of −1.8 V to −1.5 V where the impedance of the methacrylate and aniline based ultra-thin layer become capacitive at low frequency while the APTES based ultra-thin layer still shows an effective AC leakage current. This can be explained by the variations in coverage of those ultra-layer layers which affects the positive ions (probably protons) penetration, which is assumed to be responsible for the AC conductance at negative bias, onto the porous oxide where they can be transported by percolation/diffusion onto the silicon/insulator interface.

3.5. Barrier effectiveness measurements

3.5.1. Four point probe measurements

The resistivity is presented as a function of annealing time at 525 °C for each UTL (Fig. 5).

Annealing time was segmented in a way that we could examine the effect on the UTLs both in short periods of time and long.

3.5.1.1. Copper annealing over short times. According to the measured results of the short annealing time (Fig. 5a), it is shown to cause a decrease of resistivity in the samples. This is common in copper annealing due to microstructure (i.e. grain boundary, surfaces and interfaces) changes that have a large effect on resistivity. The annealing affects grain growth, increasing average grain size, reducing grain boundary effects thus causing the resistivity to decrease [29]. Furthermore, the copper is applied using vapor deposition, and it has a significant intrinsic stress due to the temperature cycle. Annealing increases the rate of diffusion in the solid allowing the material to progress towards its equilibrium state, i.e. a more stable state (crystalline) thus reducing the residual stress enclosed in the samples and improving the metal's conductivity.

A failure of any sample would had been observed if a drastic increase in resistivity. Since no catastrophic change in the resistivity was observed we can conclude that no barrier failure had been occurring during this short period of time. The only effect of the short annealing time is to cause a stress release decreasing resistivity.

The results show the same trend of resistivity in all samples- an initial decline in resistivity.

The initial resistivity of the reference sample (without the ultra-thin layer), was higher than the rest which were of very similar values. The reason for that is linked to the fact mentioned before, diffusion of copper and silicon. The difference isn't very large, since diffusion is strongly dependent on temperature. Yet, some diffusion may have occurred even before annealing creating a certain amount of silicide raising the resistivity.

3.5.1.2. Copper annealing over long times. Since no noticeable failure occurred at short times, a longer annealing was attempted (Fig. 5b). The reference sample had the most drastic rise in resistivity after an annealing of approximately 130 min. The rest of the samples showed some increase in resistivity but not as prominent as the reference.

4. Conclusions

In this paper we present a novel elevated temperature process for ultra-thin organic layers on silicon and oxides. The films' properties have been characterized by various methods: physical, electrochemical and electrical methods.

The physical methods consisted of Contact Angle (CA), Ellipsometry, and Kelvin Probe Scanning Microscopy (KPFM). A thorough and

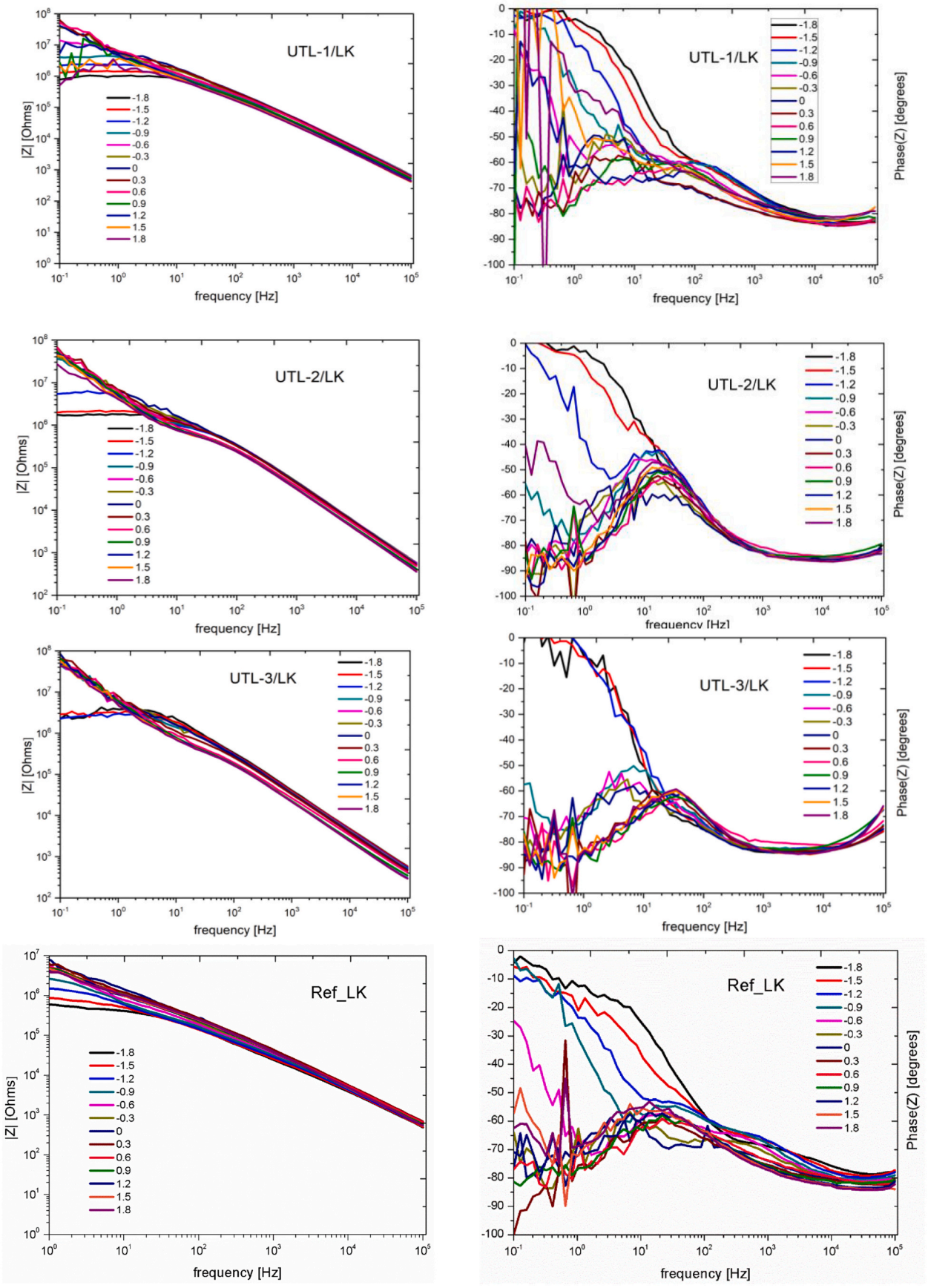


Fig. 3. EIS of ultra-thin layers (UTL) on Low-K (a) UTL −1, (b) UTL −2, (c) UTL −3 (d) reference sample without ultra-thin layers.

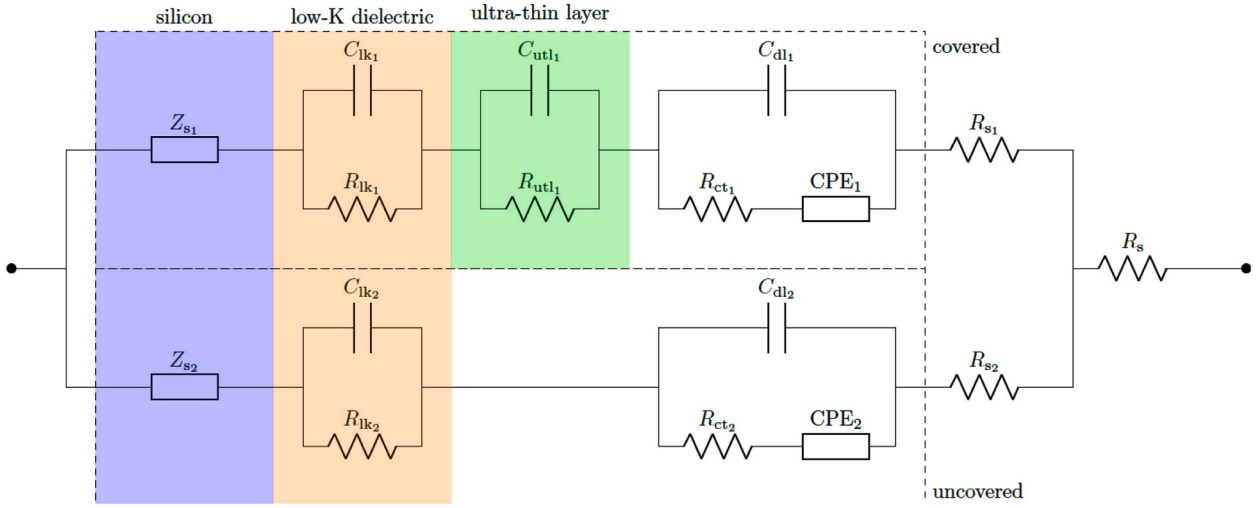


Fig. 4. Electrical model of ultra-thin layer on Low-K layer on silicon with partial coverage, x. C_{lk}: low-K capacitance, C_{utl}: ultra-thin-layer capacitance, C_{dl}: double layer capacitance, CPE: Constant phase element, R_s: serial resistance, The indices 1&2 are for the covered and uncovered regions.

Table 2
Average effective electrical coverage of ultra-thin layers on Low-K.

Ultra-thin layer (UTL)#	Ultra-thin type (Table 1)	Electrical coverage%
1	APTES-UTL/Low-K/Si	47.8
2	Methacrylate-UTL/Low-K/Si	69.9
3	Aniline-UTL/Low-K/Si	85.3

detailed description was dedicated to the electrochemical impedance spectroscopy method which can provide very useful information in relatively simple setup for in-line measurements. This method can be extended also to other ultra-low thin films; i.e. Atomic Layers Deposited or grafted Langmuir-Blodgett films. In this paper we propose to use the low frequency characteristics at accumulation to estimate the effective electrical coverage and later using that parameter to estimate the ratio between the ultra-thin layer capacitance to that of the double layer $\frac{C_{ML}}{C_{dl}}$. This method can be verified by experiments where we modify the double layer capacitance, for example by changing the electrolyte concentration.

The Electrochemical Impedance Spectroscopy (EIS) method was further utilized to estimate the effective electrical coverage of the ultra-thin layer on the porous Low-K dielectric. In this case the change in the total capacitance with and without the ultra-thin layer was very small. The breakthrough comes when we look at high negative bias, where the ultra-thin layer/Insulator/Si capacitor is in strong accumulation its porous layer dielectric capacitance is in parallel to a serial resistance, most probably due to positive ion conduction, probably protons.

Those results require some further discussion on the meaning of the electrical coverage that is discussed in this paper and how it is related to the material coverage. Coverage can be defined in absolute or relative values. Previous works on SAM surface coverage typically define material coverage in units of mol/per cm square. Materials coverage can be measured by material science surface characterization methods as well as electrochemical methods [31,32]. For example, the full coverage of ll-Mercaptoundecanoic acid (MUA on (111) Au was measured by integrating the cathodic peak due to the reductive desorption of the MUA and was found to be as 8.0×10^{-10} mol $\times$ cm^{-2} for immersion time longer than 12 h [30]. They note in that paper that this value is close to the value of 7.6×10^{-10} mol $\times$ cm^{-2} which is not far from the theoretical areal density of gold atoms assuming ideal (111) FCC surface with a unit cell as $A = \frac{16\sqrt{3}}{3}R^2$ where R is the atomic radius. This concept of material coverage in units of mol $\times$ cm^{-2} can be extended the ultra-thin films as discussed in our paper; However, there is always the issue of developing a rapid method assessing the coverage. There are many papers discussing surface material science methods and they are summarized in few classical review papers [30,31]. One of the proposed

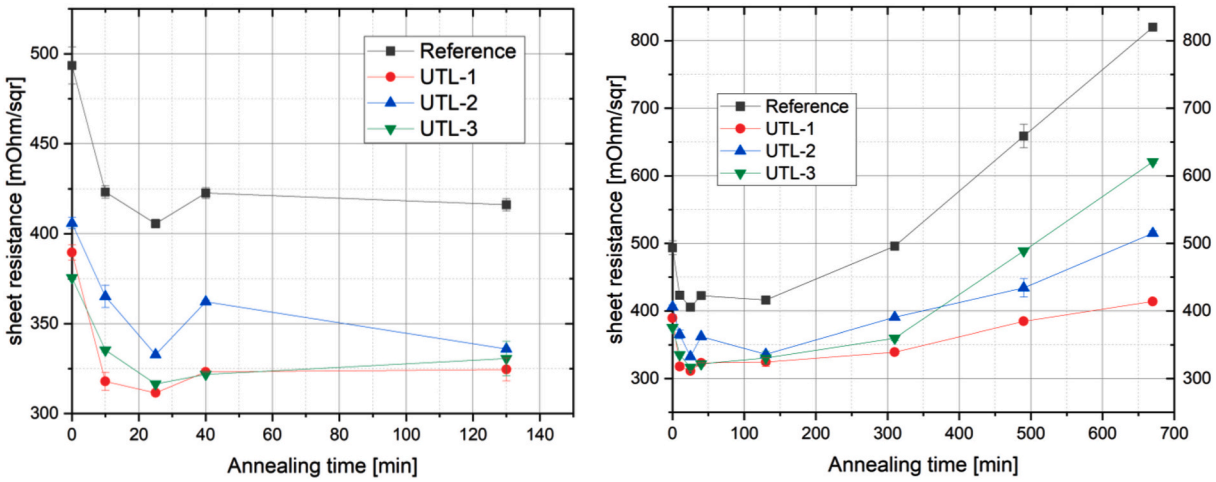


Fig. 5. Cu/barrier/Si sheet resistance after thermal annealing at 525 °C a. short periods and b. over long periods.

methods for characterizing ultra-thin layers and SAM on conductors and semiconductors is the use of electrochemical impedance spectroscopy (EIS) [32]. The effective electrical surface density coverage is derived from the equivalent electrical circuit describing the substrate/UTL/electrolyte interface (UTL: Ultra-Thin Layer). Using Randle's model [26], we can define an effective coverage from the extracted double layer capacitance, charge transfer resistance or from the constant phase element (CPE) which represents the contribution of the ion transport in the electrolyte near the electrode to the overall electrical impedance. Previous data indicated that the electrical surface coverage is different than the molecular surface coverage. It was assumed (for example [17,32,33]) that the electrical surface density is determined by pores in the UTL. Hence, it is assumed that the UTL is in general a low conduction material and the increase in conductivity is due to defects allowing the solution to be in better contact with the conductive substrate. This model assumes that the defected area has a similar model to the ideal UTL, however, with different parameters; usually higher conductivity, higher capacitance and different values for the constant phase element.

In the work presented here a similar approach can be attributed to measurements of ultra-thin layers on thick porous insulators. It is assumed that the effective electrical circuits at the uncovered regions is different than what is describing the regions where the UTL is intact.

This approach assumes taking two measurements, with and without the ultra-thin layer and comparing the results. The measurement can be on the same sample before and after the ultra-thin layer deposition or taking few exactly identical samples, deposit the UTL on few of those sample, performing the measurement and calculating the average and the standard deviations. The results indicate always on a slight decrease of the double layer capacitance after the UTL deposition, indicating on the addition of a thin insulator. However, since the UTL is very thin this decrease is small can be used to verify that there is a UTL and in many cases does not provide accurate evaluation of the surface converge. In this work we observed that if we perform the EIS under negative bias (On the substrate relative to the reference) at the low frequency range the real part in the Randle's model is affected by the SAM deposition. It is assumed that.

The charge transfer resistance is representing some electrochemical reaction at the electrode where the AC current is in phase with the alternating voltage. In this case we assume that the amount of the decrease of that conductivity is due to an increased ionic conduction in the porous material and it represents the defects, or pores in the UTL on the porous insulator. In other words, the less this UTL coverage the lower the number pores in the UTL, the closer the conductivity of the samples with the UTL to those without the UTL. It should be noted that it is still unknown how those electrically determined defects are related to copper barrier failure due to defects in the barrier.

In summary, it has been demonstrated here that the EIS method can be used to measure effective ultra-thin layer coverage, even on a relatively thick, (e.g. "much thicker than the ultra-thin layer") Low-K dielectric, if there is enough leakage which is induced at very negative bias at accumulation (for p-type substrate). We also used the effective electrical coverage as a figure of merit. However, more work is needed to understand the meaning of this electrical coverage; Specially to find it whether the effective electrical coverage is related to the actual physical coverage and the relation of both electrical and physical coverage to the barrier integrity and its failure modes. EEC value should be compared to other surface science methods (i.e. TEM, XRR etc.) that are more accurate and yield a more physically oriented value but they are slow, expensive and problematic due to the fact that ultra-thin organic barriers have similar material properties to that of Low-K dielectrics.

The barriers properties of the organic layers were studied at 525 °C for different periods of time and we conclude that all tested organic layers can serve as barrier layers for 400 min (Fig. 5). After 400 min, there was a sharp rise indicating on a degradation of the ultra-thin barriers. Out of the organic layers considered, the 3-(Trimethoxysilyl) propylmethacrylate (Meta) showed the best barrier results, indicating probably a denser ultra-thin layer as compared to the other molecules tested. Note that silane barrier deposition from the liquid phase on porous lowK materials may pose some problems and may require some special treatments [34,35] However, the EIS measurements of the ultra-thin layer that has been deposited from high flash point solvents over the porous (< 1 nm pores) LowK material had demonstrated a slight decrease in the capacitance that was attributed to the added ultra-thin layer. Further study is needed to explore such solvents on fine-pores (< 1 nm) LowK materials. One possible option is that since NMP is strongly polar ($\mu = 4.09$ D) aprotic solvent [36] with molecular size in the range of 0.5–0.8 nm and since glycerol larger diameter is about 0.6–0.7 nm those molecules are almost of the same size of the lowK pores, 0.8 nm. It is also important to study the wetting properties of those solvents. Moreover, the study presented show feasibility of ultra-thin barriers deposited form high flash point solvent; further study is needed to evaluate the UTL reliability, for example by Bias Thermal Stress test.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mee.2020.111468.

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